**This project designs and simulates a high-speed CMOS frequency divider using 65 nm process technology.**

**The circuit takes a 2 GHz input clock and produces a 1 GHz output clock, effectively dividing the frequency by two.**

**Frequency dividers are widely used in digital and communication systems to:**

**\_Reduce power consumption in slower system blocks.**

**\_Enhance timing stability and minimize synchronization errors.**

**\_Provide lower clock frequencies for control or processing units.**

**The goal is to achieve the best speed–power trade-off by designing a transistor-level D flip-flop circuit.**

**The work includes selecting a logic style (TSPC, CML, or CMOS), sizing transistors (W/L), and simulating for performance metrics like maximum frequency, power, and Figure of Merit (FoM).**

**2. CMOS Technology**

**Advantages:**

**\_Very low static power consumption.**

**\_High noise immunity and excellent scalability (65 nm → high speed, small area).**

**\_Good balance between speed and power efficiency.**

**Limitations:**

**\_Power increases with switching frequency.**

**\_Leakage currents and process variations at deep-submicron levels.**

**3. TSPC Logic**

**Advantages:**

**\_Operates at very high speed (multi-GHz).**

**\_Requires only one clock phase, reducing complexity and power.**

**\_Fewer transistors → smaller area and faster switching.**

**Limitations:**

**\_Sensitive to leakage and noise.**

**\_Cannot hold data when the clock stops.**

**Use in this project:**

**TSPC flip-flops are ideal for the divide-by-2 design, offering higher speed and lower dynamic power than static CMOS DFFs.**

**4. CMOS vs. TSPC Comparison**

**Feature: Static CMOS TSPC**

**Clock: Dual-phase (CLK, CLKb) Single-phase**

**Speed: Moderate Very High**

**Power: Moderate Lower at high speed**

**Area: Larger Smaller**

**Data Retention:Yes No**

**Use: Medium-speed designs High-speed dividers**

**5. Project Steps:**

**1. Study Theory: Review D flip-flop and frequency division principles.**

**2. Design: Build a toggle DFF (D = ¬Q) using 65 nm CMOS or TSPC logic.**

**3. Sizing: Choose optimal W/L ratios for high speed and low power.**

**4. Simulation: Verify divide-by-2 operation at 2 GHz; measure frequency, power, and FoM.**

**5. Optimization: Adjust transistor sizes and logic style for best efficiency.**

**6. Results: Present waveforms, power data, and performance discussion.**

**7. Extension (Optional): Implement divide-by-N or dual-modulus (2/3) version for PLL use**

**6. Expected Results:**

**\_Output frequency = Input / 2 (1 GHz).**

**\_TSPC design achieves higher speed with lower power.**

**\_FoM improves due to reduced switching energy.**

**\_Demonstrates effective speed–power optimization in 65 nm CMOS technology.**