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**65 nm CMOS Process Design Kit (PDK)**

This project aims to design and simulate a high-speed CMOS frequency divider using 65 nm process technology. The circuit receives a high-frequency clock input (around 2 GHz) and produces an output clock with a lower frequency, typically divided by two. Frequency dividers are fundamental components in digital and communication systems, as they generate slower clock signals from a high-speed master clock.

Lower frequencies are often required to reduce power consumption in circuit blocks that do not need to operate at maximum speed, improve overall system stability by minimizing timing errors caused by excessive clock rates, and provide suitable clock signals for different system stages such as control or processing units. In this way, the divider contributes to both energy efficiency and timing reliability across the entire system.

The project focuses on implementing digital logic principles—particularly D flip-flop–based architectures—at the transistor level using CMOS technology, achieving an optimal trade-off between speed and power efficiency. The main engineering challenge lies in choosing an appropriate high-speed logic style (e.g., TSPC, CML, or optimized CMOS), sizing transistors (W/L ratios) for high performance, and simulating the design to evaluate its maximum operating frequency, power consumption, and Figure of Merit (FoM). Optionally, the project can be extended to a programmable or dual-modulus divider (e.g., divide-by-2/3 or divide-by-8/9), which are commonly used in Phase-Locked Loops (PLLs) and frequency synthesizers for high-frequency applications.